AMENDMENT TO THE SPECIFICATION:

Please replace the paragraph found at p. 1, lines 8-24 with the following amended paragraph:

A Type Two PLL filter system has the well known form shown below in Figure 1. A charge pump circuit operates under the control of a phase/frequency detector to develop a voltage across the filter network formed by ~~resister~~ resistor (R1), and capacitor (C1 and C2) which provides the input to a voltage controlled oscillator (VCO). The poles of the filter are set by time constants t=R1(C1+C2) and t2=R1C2 and in many applications it is necessary to tune this filter network during operation, for example to compensate for process/operating changes or to change the dynamics of the PLL system during a different mode of operation. When this filter is integrated, this is often performed by changing one of the capacitor values, usually C1. However, C1 is also a parameter in the open loop gain of the PLL and changes in its value often necessitate a change in another of the gain parameters such as the charge pump current to prevent the PLL gain from also changing.